



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:

Chian-Min Richard Ho et al.

Assignee:

0IN Design Automation, Inc.

Title:

Method for automatically searching for defects in a description of a circuit

Serial No .:

09/849,005

Filing Date:

May 4, 2001

Examiner:

Frejd, Russell Warren

Group Art Unit:

2123

Docket No.:

0IN006-1C US

Confirmation No:

1848

Santa Clara, California October 10, 2003

COMMISSIONER FOR PATENTS P.O. BOX 1450 ALEXANDRIA VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97(c)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, §1.97 and §1.98, the Applicants submit for consideration in the above-identified patent application the documents listed on the accompanying Forms PTO-1449. The Forms PTO-1449 are submitted in two parts, namely Part A of 3 sheets and Part B of 24 sheets. Copies of 28 documents cited in Part A are also submitted herewith (but references 9, 10 and 11 are not being submitted and the Examiner is requested to obtain them from the USPTO files of the parent application). The Examiner is requested to make all these documents of record. Applicants would appreciate the Examiner initialing and returning the all the Forms PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement is submitted pursuant to 37 CFR §1.97(c) as it is after receipt of a first Office Action on the merits but before mailing of a final Action or Notice of Allowance. Accordingly, a fee is required pursuant to 37 CFR §1.17(p). A Fee Transmittal form (PTO/SB/17) is attached to this submission.

In addition, Applicants submit for the Examiner's consideration the following list of co-owned patents and application, cited by serial number, first named inventor and

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SILICON VALLEY
PATENT GROUP LLP

ssion College Blvd. Suite 360 Santa Clara, CA 95054 (408) 982-8200 FAX (408) 982-8210

Application No. 09/849,005

filing date. The Applicants presume that the Examiner has access to and will review the coowned patents and applications and the files thereof for any office actions, amendments or other materials that may be relevant to the patentability of the claims of the present application. For any such U.S. patent application(s) that are currently pending, the Applicants further presume that the Examiner will consider any future office actions, amendments or other materials in the file thereof that may be relevant to the patentability of the claims herein.

If the Applicants' understanding in this regard is not correct, please notify the undersigned so that copies of any such documents can be submitted to the Examiner

	Serial No.:	First Named Inventor	Filing Date:
1.	08/955,329	Ly et al.	10/20/1997
2.	09/635,598	Ly et al.	8/9/2000
3.	10/348,116	Ly et al.	1/20/2003
4.	08/954,765	Ho et al.	10/20/1997

The information contained in this Information Disclosure Statement under is to the best of my knowledge and is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Via Express Mail Label No. ER 205 704 792 US

Respectfully submitted,

Omkar K. Suryadevara Attorney for Applicants

Reg. No. 36,320

SILICON VALLEY
PATENT GROUP LLP

2350 Mission College Blvd. Suite 360 Santa Clara, CA 95054 (408) 982-8200 FAX (408) 982-8210

Sheet 1 of 24 U.S. Department of Commerce, Patent and Trademark Office Atty Docket No. Serial No. 01N006-1C US 09/849,005 ON DISCLOSURE STATEMENT BY APPLICANT Applicants: Chian-Min Ho et al. Use several sheets if necessary) Filing Date Group MAY 4, 2001 2123 U.S. Patent Documents *Examiner Document Filing Date Initial Number Date Name Class Subclass If Appropriate 5,555,270 AA 9/10/96 Sun et al. 371 27 AB5,630,051 5/13/97 Sun et al. 395 183.08 AC 5,600,787 2/4/97 Underwood et al. 395 183.06 AD 5,623,499 4/22/97 Ko et al. 371 22.1 **AE** 5,654,657 8/5/97 Pearce 327 163 AF 5,729,554 3/17/98 Weir et al. 371 27 Foreign Patent Documents Translation Document Date Country Class Subclass Yes No AG AH OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Windley, Phillip J., "Formal Modeling and Verification of Microprocessors", IEEE Transactions on ΑI Computers, Vol. 44, No. 1, January 1995, pp. 54-72. Clarke, E. M., et al., "Efficient Generation of Counterexamples and Witnesses in Symbolic Model AJ Checking", 32nd Design Automation Conference, June 12-16, 1995, pp. 427-432. Silburt, Allan, et al., "Accelerating Concurrent Hardware Design with Behavioral Modelling and System AK Simulation", 32nd Design Automation Conference, June 12-16, 1995, pp. 528-533. Jones, Robert B., et al., "Efficient Validity Checking for Processor Verification", IEEE International AL Conference on Computer-Aided Design, November 5-9, 1995, pp. 2-6. Clarke, Edmund M., et al., "Model Checking and Abstraction", ACM Press Conference Record of the AM Nineteenth Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, January 19-22, 1992, pp. 343-354. Aagaard, Mark D., et al, "The Formal Verification of a Pipelined Double-Precision IEEE Floating-Point AN Multiplier", 1995 IEEE/ACM International Conference on Computer-Aided Design, November 5-9, 1995, pp. 7-10. Clarke, E. M., "Representing Circuits More Efficiently in Symbolic Model Checking", 28th ACM/IEEE AO Design Automation Conference, June 17-21, 1991, pp. 403-407. Examiner Date Considered *EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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